Single Electron Tunneling Technology based Level Sensitive SR Latch Circuit for Next Generation Novel Bios Architecture

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***Abstract*—Downscaling of the minimum feature size of CMOS transistor has been the basis for advancement in the ultra large integration technology for long years. But by no means it is a never-ending process. The Single Electron Tunneling (SET) technology has created high expectations for post CMOS era as it is compatible for designing low power consuming nano-scaled device that posses high integration density. The tunnel junction of the SET circuits is the key basis that controls the movement of individual electrons. The present work demonstrates a hypothetical approach to design a Single Electron Device (SED) based commercially viable logic circuit to be incorporated in next generation ICs.**

Keywords- Single Electron Tunneling; Single Electron Device; e-beam lithography; tunnel junctions; Coulomb Blockade

I. INTRODUCTION

Downscaling of electronic device sizes is fundamental for continuing the progress of very large scale ICs. MOSFETs, are reckoned as the most prevalent electron devices for VLSI applications, and thus shrinking of MOSFET size [1-3] is optimum for the development of the semiconductor industry. The driving force accounted for the radiance in electronic industry is Moore's Law. As stated by Sir. G. Moore - the transistor density of a single chip doubles within the span of only 18 months; the cost and power of the chip is reduced considerably [4]. Dennard in his classic theory [5] in late 1970's pointed out that simple dimension shrinkage with supply voltage if reduced in a relatively slow pace can enhance the transistor density as well as improve the performance simultaneously. However, the reality is that the power dissipation has also increased proportionately. The fact is that if it remains unchanged, then the power density of chip is soon likely to exceed the value in a nuclear reactor or equal to the value on the surface of sun [6,7]. With the power dissipation ripens to serious hindrance of technological advancement, novel technologies are prerequisite to solve the power dissipation problems along with short channel effect, leakage phenomena and performance degradation like problems. In this 'More Than Moore' technological aspect SET based SEDs are opted as new horizon of future commercial electronics.

The extensive sophisticated advanced e-beam lithography technique revolutionized the age old fabrication technique for device miniaturization [8]. Along with this SET technology paved his way into the nanoelectronics. The intrinsic worthiness of SET technology is the potentiality to carry one electron singly i.e., merely a single electron is enough to toggle on and off states of a SET; whereas, transistors in conventional CMOS based microelectronics hang on on millions of electrons to perform the same transition [9-12].

The low power operational characteristic of SET controls the instability and reliability problem. The speed power product lies just underneath the quantum limit set by the Heisenberg's uncertainty principle. The processing speed is approximately same to the electronic speed whereas the exquisite sensitivity is of five orders of magnitude when compared to conventional solid-state MOSFET transistors. Besides low power consuming operations; comparison between SET and CMOS revealed that (1) the integration density remains much higher than the present VLSI/ULSI chips; (2) the propagation delay is of 4ns, which is $1/3^{rd}$ of the propagation delay of the conventional gates that take 12ns for the same device operation (3) the execution time required is nearly one third of the conventional logic based circuits and (4) the speed efficiency improves to 300% in respect to CMOS transistors [13-17].

SET exhibits incredible viability and potentiality. There has been reports of extensive research to develop specific applications of SETs in Defense applications (for unmanned and remote areas), Space Technologies (such as space vehicles), medical applications (such as space-maker battery) etc. The research criteria in such applications are concentrated on minimum power for maximum battery lifetime. Remarkably, the power savings remains the highly decisive factor for most portable application. In contrast for low power consuming device the size of the device can be reduced considerably. These talents of SET show enormous possibility for applications in modern technological era. Researchers now tend to employ this technology in every sphere of life. Here the authors report a novel design of Level Sensitive SR Latch based on SET technology with the aim to implement the same logic in SED made IC. Subsequently the orthodox theory of SET is bestowed along with some logical realizations using

SETs and finally the Level Sensitive SR Latch circuit is modeled.

II. THE ORTHODOX THEORY OF SET TECNOLOGY

A. SET Structure

As represented in Figure 1, two tunnel junctions positioned in series (known as a Coulomb-island) forms the SET. Electrons are permitted to enter by tunneling through one of these insulators. The device configuration of SET is quite identical with the ordinary Field Effect Transistor (FET) having three terminals; i.e., the outside terminal of each tunnel junction labeled as "source" and "drain"; and the "gate" terminal that are capacitively coupled to the node between the two tunnel junctions. The capacitor performs as a third tunnel junction, but from the constructional perspective it is much thicker than the others so that no electrons can tunnel through it. The capacitor is subjected to provide the path of setting the electric charge on the Coulomb Island [18-22].

B. Coulomb Blockade Structure

The electrical potential of the Coulomb Island as projected is tuned using a third electrode, known as the gate. Structurally, it is capacitively coupled to the island. In the blocking state the accessible energy levels are far beyond the tunneling range of the electron on the source contact. All energy levels on the island are occupied with lower energy electrodes. The substitute is to apply positive voltage to the gate electrode and thereby the energy levels of the island electrode are lowered. The electron (e^1.) can tunnel onto the island (e^2.), occupying a previously vacant energy level. From there it can tunnel onto the drain electrode (e^3.) but it shows much inelasticity to scatter and reach the drain electrode Fermi level (e^4.). The energy levels of the island electrode shown in the Figure. 2 are evenly spaced (i.e., apart ΔE). This increases the self-capacitance C of the island, given by $C=e^2/\Delta E$ [23,24].

C. Passing of Electrons through Tunnel Junction

The Tunneling of an electron occurs from point to point of a tunnel junction to the opposite end point of the tunnel junction; thereby the charge distribution of that particular circuit varies. The controlling strategy is that we require Coulomb Energy E_C to charge an island with an electron where $E_C=e^2/(2C)>K_BT$; only if C is the overall capacitance of an island and K_B is Boltzmann's constant ($K_B=1.38\times10^{-34}$ J/K). In case this Coulomb Energy is greater than the available thermal energy, the movement of electrons can be controlled by controlling the available energy supplied by voltage source as shown in Figure 3. [25-28].

D. Single Electron Circuits

The simple notion of operation is that if an electron approaches at point 'A' and simultaneously if the pulse i.e., $\Phi_{n-1}>5$mV is applied then the electron passes the tunnel junctions (J1 and J3) to C or E as in Figure 4. Even though, tunneling is subjected to the condition of the Coulomb energy [$E_c=e^2/(2C)$] plus the applied energy must be greater than the potential height of the barrier energy of junction(s) J1or J3. Thus, the electron trails the path ABCD or ABEF as long as the signal $X_i>5$mV and the corresponding total energy i.e., Coulomb energy plus the applied energy is greater than static potential junction energy of J2 or J4. This route ABCD or ABEF is thought of '1'-branch or '0'-branch. This acknowledged procedure is the basis of designing several Tunnel Junction made Digital Logic Circuits [29-34].

III. LOGIC GATE DESIGN USING SET

Before industrial production of SET based circuits, it is utmost essential to explore and exploit all the intrinsic qualities of SETs in a broader way to develop fundamental logic gates in a comprehensive manner. Several attempts have been reported so far in this regard [35-38]. Keeping pace with conventional logics, SETs fundamentally are a greater successor in next generation nano ICs. For real time applications SET based various logic gates have been under in-depth research [39-42]. Such SET based AND, OR, NOT, NOR and NAND gates are shown below in Figure 5, 6, 7, 8 and 9 respectively.

Authors here accumulate these sophisticated designed gates to shape the newly proposed unconventional logic design of level sensitive SR latch.

IV. SET LOGIC GATE BASED LEVEL SENSITIVE SR LATCH DESIGNING

Before further deep penetrating into the main topic of SET made exclusive latches for next generation novel bios architecture, the authors tally the associated problems of ordinary SR latches. The problems are enumerated in the following sections categorically. Finally the empirical results are summed up to design the novel SET based SR latch nano IC.

A. Problems and Anticipated Solutions of conventional SR latch

Does not the conventional circuit of SR latch with cross-coupled NOR gates perform as per scheduled? What happens if S=1 & R=1 simultaneously and both are released to 0? The answer lies in the uncertainty i.e., we don't know what value of Q (output) will be. Q is supposed to oscillate depending on the slightly longer path of the NOR gates than the other making it 0 or 1 eventually. The attributed problem considered here is not just one of a user pressing two buttons at the same time but also the same situation arises if SR inputs are resulted from a circuit that supposedly never sets S=1 and R=1 at the same interval. It also originates due to different delays of different paths.

One probable approach is to add a clock enabled signal to the inputs of SR latch which changes the state of S & R only when it is in zero state. Otherwise the input signal to the SR latch circuit is never set SR=11, except momentarily due to path delays. To maintain stability –

i. It is required to change clock signal to 1 only after sufficient time for S and R to be stable.

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ii. Simultaneously when clock signal is enabled i.e., it becomes 1, the stable S and R value passes through the two AND gates placed earlier to the SR latch's S1 and R1 inputs.

The outcomes are – (a) ensures that never S and R becomes 1 and 1 (b) it stabilizes the state i.e., it operates only when clock is set to 1 and (c) it stores the bit.

V. THE SET BASED LEVEL SENSITIVE SR LATCH IC

An attempt to design the entire Level Sensitive SR Latch required painstaking and restless effort using SET logic. The all-inclusive detailed structure is enunciated in Figure 10. The modus operandi of the circuit is simple but robust because of its intrinsic quality.

The empirical design is thoroughly scrutinized using Monte Carlo based simulation platform. The outcomes of the model are of better acceptability and the process undoubtedly has a greater proximity in being realized in an on-chip platform. Other step by step analysis of the circuit is not shown here due to space limitations but the vital statistics are penned down in the following sections to study its effectiveness in the post CMOS era.

A. A Comparative Study of CMOS based and SET based Level Sensitive SR Latch Circuit

The Table.1 corresponds to the comparative study of the Level Sensitive SR Latch circuit keeping in mind that the most efficient fabrication technology is adapted for both Transistor-Transistor Logic and Single Electron Transistor Logic. Other careful thoughts include that in both the cases simplicity is given the first criteria to make the circuit cost effective.

Study rendered that in all state of affairs the SET based Level Sensitive SR Latch Circuit possess larger aptness than conventional CMOS based circuits. The projected future SET based IC is not only very low power consuming architecture but it can provide result at a quicker speed. Thus a very high-speed computation is certainly attained with this design of newly proposed SET based Level Sensitive SR Latch IC. The power dissipation as originated for switching a single bit is of few μW which is noticeably minute when compared to conventional devices. It comprises higher prospect of providing much more component density thereby reducing the future IC sizes. Besides, other phenomenal distinctiveness, this SET based Level Sensitive SR Latch circuit is quite faster than any conventional CMOS based circuit.

TABLE I.

The Comparative Study of CMOS vs. SET				
Circuit Name	***Propagation Delay time per Gate***	***Faster speed***	***Power dissipation per Gate***	***Consume Power***
CMOS	12 ns	1	0.01 / 10-12 mW	1
SET	6 ns	2	~1μW	$1/10^3$

Some approximate but much proximity to the actual values are indexed.

VI. CONCLUSION

The Single Electron Tunneling technology is fabricated with the composite fundamental concept of manipulating electrons at a large scale and the robust effects of the electronic charge discreteness. Its unmatched magnitude is amplified periodically with size reduction. In this modeling endeavor, the single charge is proficiently and resourcefully incorporated to manipulate and control the correlated electron tunneling in small capacitance structure. The contemporary era demands superiority by including low power consuming, nano dimensional, longer battery life and easy portable consumer electronics into daily life which can be achieved only if advantageous power consumption technique can be adopted and if the size can be absolutely reduced for easy portability like considerations. In these circumstances SET technology has positioned itself in a driving seat. Further the aspiring logical operations when realized by SET technology, creates greater prospect in future SET based Logic Circuits. Sophisticated mankind is waiting eagerly to adopt several decision-making technologies and thus this quest to commercialize the SET technology in a broader way has moved the Scientists and Researchers to devote themselves in hardware implementation of such technologies.

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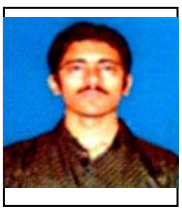
Mr. R. S. Bandyopadhyay is a final year student of B.Tech in Electrical Engineering Department of Camellia School of Engineering and Technology, West Bengal, India.



Mr. S. Dan is a final year student of B.Tech in Electrical Engineering Department of Camellia School of Engineering and Technology, West Bengal, India.

VII. LIST OF FIGURES

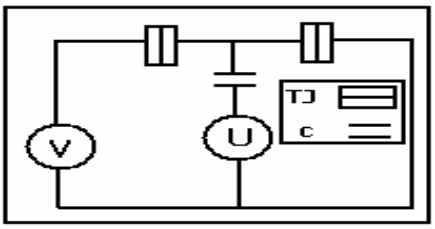


Figure 1. SET structural view

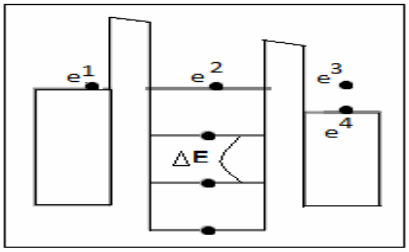


Figure 2. Energy Levels of the Island Electrode Coulomb Blockade

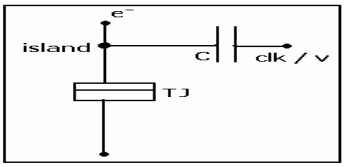


Figure 3. Passing of electrons in Tunnel Junction

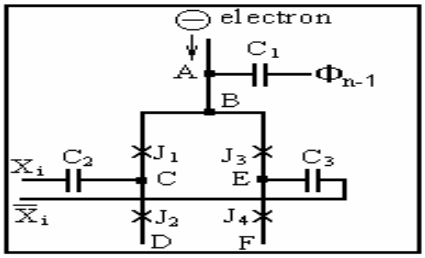


Figure 4. Electron flow path

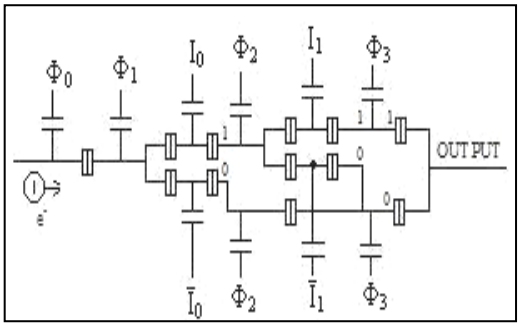


Figure 5. 2 input AND Gate usin g SET

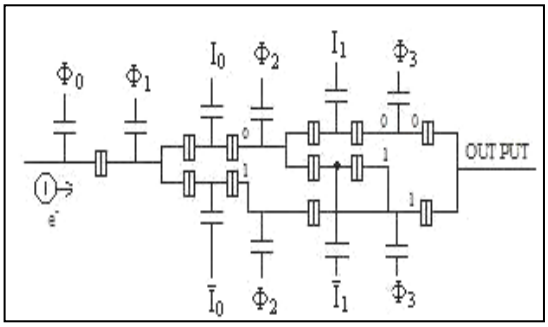


Figure 6. 2 input OR Gate using SET

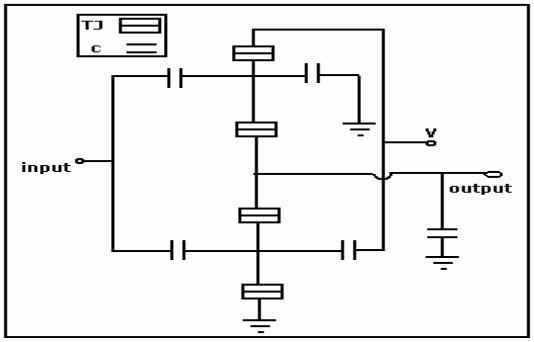


Figure 7. 2 input NOT Gate using SET

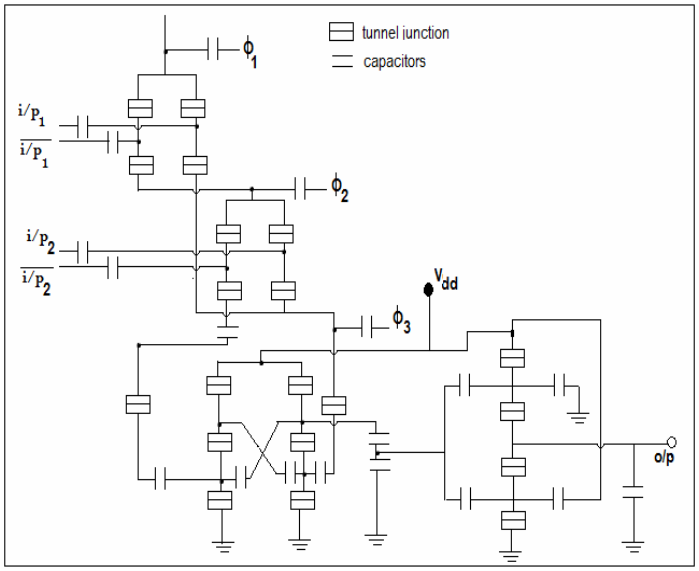


Figure 8. 2 input NOR Gate using SET

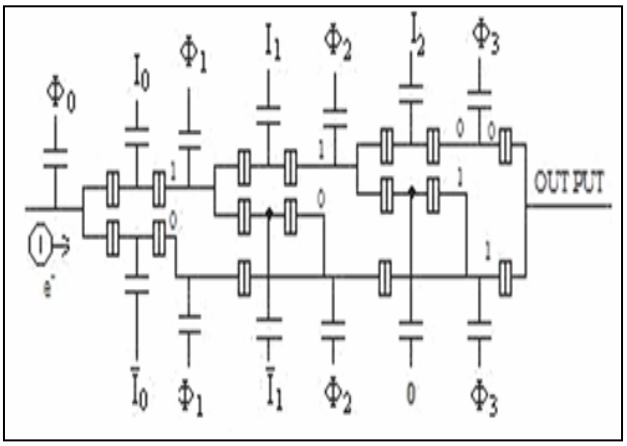


Figure 9. 2 input NAND Gate using SET

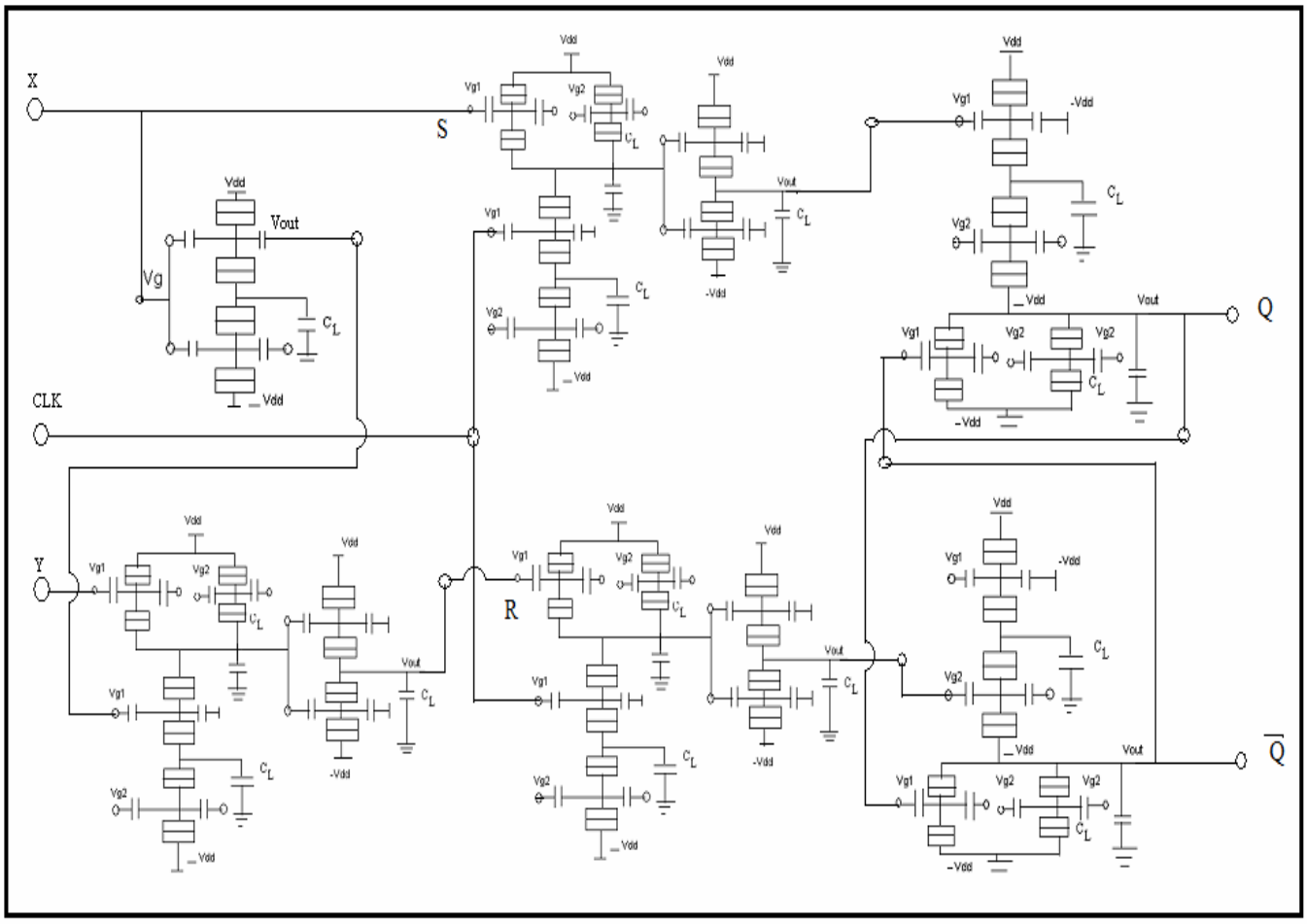


Figure 10. SET Logic Gate Based Level Sensitive SR Latch IC